Document number 2006022

PHY Silicon Network Interoperability Test Specification

August 24, 2007

Sponsored by:

1394 Trade Association

Accepted for publication by

This draft specification has been accepted by the
1394 Trade Association Board of Directors

Abstract

The IEEE-1394 PHY Silicon Network Interoperability Test is designed to verify IEEE-1394 PHY silicon implementations in various configurations

Keywords

IEEE 1394, Serial Bus, …

1394 Trade Association Specification

1394 Trade Association Specifications are developed within Working Groups of the 1394 Trade Association, a non-profit industry association devoted to the promotion of and growth of the market for IEEE 1394-compliant products. Participants in Working Groups serve voluntarily and without compensation from the Trade Association. Most participants represent member organizations of the 1394 Trade Association. The specifications developed within the working groups represent a consensus of the expertise represented by the participants.

Use of a 1394 Trade Association Specification is wholly voluntary. The existence of a 1394 Trade Association Specification is not meant to imply that there are not other ways to produce, test, measure, purchase, market or provide other goods and services related to the scope of the 1394 Trade Association Specification. Furthermore, the viewpoint expressed at the time a specification is accepted and issued is subject to change brought about through developments in the state of the art and comments received from users of the specification. Users are cautioned to check to determine that they have the latest revision of any 1394 Trade Association Specification.

Comments for revision of 1394 Trade Association Specifications are welcome from any interested party, regardless of membership affiliation with the 1394 Trade Association. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments.

Interpretations: Occasionally, questions may arise about the meaning of specifications in relationship to specific applications. When the need for interpretations is brought to the attention of the 1394 Trade Association, the Association will initiate action to prepare appropriate responses.

Comments on specifications and requests for interpretations should be addressed to:

Editor, 1394 Trade Association
315 Lincoln, Suite E
Mukilteo, Wash 98275
USA

1394 Trade Association Specifications are adopted by the 1394 Trade Association without regard to patents which may exist on articles, materials or processes or to other proprietary intellectual property which may exist within a specification. Adoption of a specification by the 1394 Trade Association does not assume any liability to any patent owner or any obligation whatsoever to those parties who rely on the specification documents. Readers of this document are advised to make an independent determination regarding the existence of intellectual property rights, which may be infringed by conformance to this specification.

Published by
1394 Trade Association
315 Lincoln, Suite E
Mukilteo, Wash 98275 USA

Printed in the United States of America

Contents

Figures

Annexes

Foreword

This specification defines the IEEE-1394 PHY Silicon Network Interoperability Test and is designed to verify IEEE-1394 PHY silicon implementations in various configurations.

There is one annex in this specification. Annex A is normative and part of this specification.

This specification was accepted by the Board of Directors of the 1394 Trade Association. Board of Directors acceptance of this specification does not necessarily imply that all board members voted for acceptance. At the time it accepted this specification, the 1394 Trade Association. Board of Directors had the following members:

Eric Anderson, Chair
Zeph Freeman, Vice-Chair
Dave Thompson, Secretary

Organization Represented *Name of Representative*
.....
The Compliance and Interoperability Working Group, which developed and reviewed this specification, had the following members:

Richard Mourn, Chair

Revision history

Revision 0.4 (March 29, 2007)

Added Interoperability Test Chapter.

Edited to show root indication for a topology figures.

Added LTN replacement configuration option were appropriate.

Revision 0.5 (May 4, 2007)

Added Signal Integrity Test Chapter.

Clarified isochronous and asynchronous test duration in Test Procedures chapter.

Clarified what Test Nodes shall the Port Connection tests be run.

Revision 0.6 (June 18, 2007)

Accepted all changes from Revision 0.5

PHY Silicon Network Interoperability Test Specification

1 Scope and purpose

1.1 Scope

The IEEE-1394 PHY Silicon Network Interoperability Test is designed to verify IEEE-1394 PHY silicon implementations in various configurations relative to: data/strobe (DS) only, beta only, hybrid bus, root, not root, junior border, not junior border, senior border, not senior border, proxy root, and not proxy root all while being stressed with asynchronous and isochronous traffic. In addition, functional areas such suspend/resume, disable/enable, and standby/restore are tested at a high level.

This test is not a low level compliance test of each PHY facility or function. In addition, it does not test the analog signal quality of the PHY silicon.

The topologies specified in this document assume a 3 port PHY. For PHYs having less than 3 ports some tests do not apply. For PHYs having more than 3 ports the tests can be extended to test all ports.

1.2 Purpose

IEEE-1394's PHY Silicon is integral to overall IEEE-1394 device interoperability. PHY silicon, having passed this test, will have a strong probability of being interoperable with other PHY silicon that has passed this test.

2 Normative references

2.1 Reference scope

The specifications and standards named in this section contain provisions, which, through reference in this text, constitute provisions of this 1394 Trade Association Specification. At the time of publication, the editions indicated were valid. All specifications and standards are subject to revision; parties to agreements based on this 1394 Trade Association Specification are encouraged to investigate the possibility of applying the most recent editions of the specifications and standards indicated below.

2.2 Approved references

The following approved specifications and standards may be obtained from the organizations that control them.

IEEE Std 1394-1995, Standard for a High Performance Serial Bus

IEEE Std 1394a-2000, Standard for a High Performance Serial Bus—Amendment 1

IEEE Std 1394b-2002, Standard for a High Performance Serial Bus—Amendment 2

1394 Trade Association, Base 1394 Test Suite Definition with Extension for 1394b

Throughout this document, the term “IEEE 1394" shall be understood to refer to IEEE Std 1394-1995 as amended by IEEE Std 1394a-2000 and IEEE Std 1394b-2002.

2.3 References under development

At the time of publication, the following referenced specifications and standards were under development.

2.4 Reference acquisition

The references cited may be obtained from the organizations that control them:

1394 Trade Association, 1560 East Southlake Blvd, Suite 242, Southlake, TX 76092 USA; (817) 416-2200 / (817) 416-2256 (FAX); http://www.1394ta.org/

American National Standards Institute (ANSI), 11 West 42nd Street, New York, NY 10036, USA; (212) 642-4900 / (212) 398-0023 (FAX); http://www.ansi.org/

Institute of Electrical and Electronic Engineers (IEEE), 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA; (732) 981-0060 / (732) 981-1721 (FAX); http://www.ieee.org/

In addition, many of the documents controlled by the above organizations may also be ordered through a third party:

Global Engineering Documents, 15 Inverness Way, Englewood, CO 80112-5776; (800) 624-3974 / (303) 792-2192; http://www.global.ihs.com/

3 Definitions and notation

3.1 Definitions

3.1.1 Conformance

Several keywords are used to differentiate levels of requirements and optionality, as follows:

3.1.1.1 expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this specification. Other hardware and software design models may also be implemented.

3.1.1.2 ignored: A keyword that describes bits, bytes, quadlets, octlets or fields whose values are not checked by the recipient.

3.1.1.3 may: A keyword that indicates flexibility of choice with no implied preference.

3.1.1.4 reserved: A keyword used to describe objects (bits, bytes, quadlets, octlets and fields) or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other specifications. A reserved object shall be zeroed or, upon development of a future specification, set to a value specified by such a specification. The recipient of a reserved object shall ignore its value. The recipient of an object defined by this specification as other than reserved shall inspect its value and reject reserved code values.

3.1.1.5 shall: A keyword that indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this specification.

3.1.1.6 should: A keyword that denotes flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “is recommended.”

3.1.2 Glossary

The following terms are used in this specification:

3.1.2.1 definition: Press ENTER to create a subsequent numbered definition paragraph …

3.1.3 Abbreviations

The following are abbreviations that are used in this specification:

TN – Generic Test Node

PUT – PHY under test

(R) – Root

BTN – Beta Test Node

DTN – DS Test Node

LTN – Beta PHY with Legacy Link (Maximum Speed is S400)

4 Test Overview (informative)

The tests defined in this document are divided into the following areas:

- Signal Integrity Tests
- Small Topology Tests
- Large Topology Tests
- Interoperability Tests
- Port Connection Tests

All test procedures for all areas are defined in the Test Procedures chapter.

The Base 1394 Test Suite Definition with Extensions for 1394b defines a set of signal integrity tests. This specification requires the PHY silicon provider to execute the appropriate tests for the set. This approach allows the PHY silicon provider the opportunity to test their implementation in an environment they feel is optimal for signal integrity. The Base 1394 Test Suite test is focused on end product testing and may not provide an optimal environment for the PHY silicon.

The small topology tests are used to verify the correct operation of the PHY Under Test (PUT) in all possible operating modes (examples: root, parent and child, child only, senior border, etc…). While in each mode of operation the PUT is stressed with asynchronous and isochronous data. Of course if the PUT doesn't support the mode of operation then the test is not required.

The large topology tests are used to verify the correct operation of the PHY Under Test (PUT) in topologies containing many repeat opportunities (hops). These tests are defined to expose any repeat and arbitration timing issues the PUT might have.

The interoperability tests utilize some of the small topology configurations and test procedures to verify the PHY Under Test (PUT) interoperability with a few other PHY silicon implementations.

The port connection tests are used to verify the high level functionality of the PHY Under Test (PUT) regarding suspend/resume, disable/enable and standby and restore. While this test does not verify the specific detail of each it does verify that the high level interoperability exists.

5 Signal Integrity Testing

This test specification requires the signal integrity tests defined in the Base 1394 Test Suite Definition with Extension for 1394b. The following sections apply:

If the device supports Data Strobe signaling section 4.3 Data Strobe (DS) Testing applies.

If the device supports Beta signaling section 4.4 Beta Testing applies.

6 Small Topology Tests

The following small topology tests are designed to verify the PHY Under Test's (PUT) operation in all possible situations. For Data Strobe (DS) and Beta only PHY's the number of topologies that apply are limited. For Bilingual port PHYs not supporting a legacy (IEEE-1394a-2000) PHY/Link interface more tests apply; however, for PHY's supporting both IEEE-1394a and b PHY/Link interfaces the most combinations apply. The test configurations are grouped based on PUT type (DS or Beta) and then based on the device types connected to PUT.

6.1 Beta Only Topology Tests (Configurations 1-4)

The tester may choose to create the specified topologies manually rather than using the disable method described below.

1) Connect configuration as shown in 6.5, Configuration 3.
2) Disable all ports except the port under test to create Configuration 1. Force PUT to be root.
3) Execute **Point-to-Point Test Procedure** and record results.
4) Disable all ports except the port under test to create Configuration 2. Force BTN to be root.
5) Execute **Point-to-Point Test Procedure** and record results.
6) If PUT has two or more ports execute the following.
7) Enable ports to create Configuration 3. Force PUT to be root.
8) Depending on Num_Ports execute test procedure and record results :
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.
9) Enable ports to create Configuration 4. Force BTN to be root.
10) Depending on Num_Ports execute test procedure and record results :
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.

6.2 DS Only Topology Tests (Configurations 5-8)

The tester may choose to create the specified topologies manually rather than using the disable method described below.

1) Connect configuration as shown in 6.5, Configuration 7.
2) Disable all ports except the port under test to create Configuration 5. Force PUT to be root.
3) Execute **Point-to-Point Test Procedure** and record results.
4) Disable all ports except the port under test to create Configuration 6. Force BTN to be root.
5) Execute **Point-to-Point Test Procedure** and record results.
6) If PUT has two or more ports execute the following.
7) Enable ports to create Configuration 7. Force PUT to be root.
8) Depending on Num_Ports execute test procedure and record results :
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.
9) Enable ports to create Configuration 8. Force BTN to be root.
10) Depending on Num_Ports execute test procedure and record results :
    c. Num_Ports = 2: **3 Node Test Procedure**.
    d. Num_Ports > 2: **4 Node Test Procedure**.

6.3 Hybrid Bus Topology with Beta Link Tests

6.3.1 Configuration 9 and 10

1) Connect configuration as shown in 6.5, Configuration 9.
2) Force PUT to be root.
3) Execute **3 Node Test Procedure** and record results.
4) Force BTN to be root, Configuration 10.
5) Execute **3 Node Test Procedure** and record results.

6.3.2 Configuration 11 and 12

1) Connect configuration as shown in 6.5, Configuration 11.
    a. If PUT is 2 port device then remove one LTN.
2) Force PUT to be root.
3) Depending on Num_Ports execute test procedure and record results:
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.
4) Force LTN to be root as shown in 6.5, Configuration 12 .
5) Depending on Num_Ports execute test procedure and record results:
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.

6.3.3 Configuration 13

1) Connect configuration as shown in 6.5, Configuration 13.
    a. If PUT is 2 port device then remove one BTN that is directly connected to PUT.
2) Force LTN to be root.
3) If PUT has two or more ports execute the following.
    a. Num_Ports = 2: **4 Node Test Procedure**.
    b. Num_Ports > 2: **5 Node Test Procedure**.

6.3.4 Configuration 14 and 15

1) Connect configuration as shown in 6.5, Configuration 14.
    a. If PUT is 2 port device, test doesn't apply.
2) Force LTN to be root.
3) Execute **4 Node Test Procedure** and record results.
4) Force DTN to be root, Configuration 15.
5) Execute **4 Node Test Procedure** and record results.

6.3.5 Configuration 16

1) Connect configuration as shown in 6.5, Configuration 16.
    a. If PUT is 2 port device, test doesn't apply.
2) Test port n (where n starts with 0 and increments to Num_Ports - 1).
3) Force BTN connected LTN to be root.
4) Execute **5 Node Test Procedure** and record results.

6.3.6 Configuration 17 and 18

1) Connect configuration as shown in 6.5, Configuration 18.
    a. If PUT is 2 port device then remove one BTN.
2) Force PUT to be root.
3) Depending on Num_Ports execute test procedure and record results:
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.
4) Force BTN to be root.
5) Depending on Num_Ports execute test procedure and record results:
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.

6.4 Hybrid Bus Topology with Beta Link Tests

6.4.1 Configuration 19, 20 and 21

The tester may choose to create the specified topologies manually rather than using the disable method described below.

1) Connect configuration as shown in 6.5, Configuration 21.
2) Disable all ports except the port under test to create Configuration 19. Force PUT to be root.
3) Execute **Point-to-Point Test Procedure** and record results.
4) Disable all ports except the port under test to create Configuration 20. Force BTN to be root.
5) Execute **Point-to-Point Test Procedure** and record results.
6) If PUT has two or more ports execute the following.
7) Enable ports to create Configuration 21. Force BTN to be root.
8) Depending on Num_Ports execute test procedure and record results:
    a. Num_Ports = 2: **3 Node Test Procedure**.
    b. Num_Ports > 2: **4 Node Test Procedure**.

6.4.2 Configuration 22 and 23

The tester may choose to create the specified topologies manually rather than using the disable method described below.

1) Connect configuration as shown in 6.5, Configuration 23.
2) Disable LTN port connected to BTN
3) Force LTN to be root as shown in 6.5, Configuration 22.
4) Execute **Point-to-Point Test Procedure** and record results.
5) Enable LTN port connected to BTN and force BTN to be root, Configuration 23.
6) Execute **3 Node Test Procedure** and record results.

6.4.3 Configuration 24

1) Connect configuration as shown in 6.5, Configuration 24.
    a. If PUT is 2 port device, test doesn't apply.
2) Force LTN to be root.
3) Execute **4 Node Test Procedure** and record results.

6.4.4 Configuration 25

1) Connect configuration as shown in 6.5, Configuration 25.

   a. If PUT is 2 port device, test doesn't apply.
2) Force BTN to be root.
3) Execute **4 Node Test Procedure** and record results.

6.4.5 Configuration 26, 27 and 28

The tester may choose to create the specified topologies manually rather than using the disable method described below.

1) Connect configuration as shown in 6.5, Configuration 28.
   a. If PUT is 2 port device, test doesn't apply.
2) Disable LTN port to BTN to create Configuration 26.
3) Force LTN to be root.
4) Execute **4 Node Test Procedure** and record results.
5) Force DTN to be root, Configuration 27.
6) Execute **4 Node Test Procedure** and record results.
7) Enable LTN port to BTN to create Configuration 28.
8) Force BTN connected LTN to be root.
9) Execute **5 Node Test Procedure** and record results.

6.4.6 Configuration 29 and 30

1) Connect configuration as shown in 6.5, Configuration 29.
2) Force PUT to be root.
3) Depending on Num_Ports execute test procedure and record results:
   a. Num_Ports = 2: **3 Node Test Procedure.**
   b. Num_Ports > 2: **4 Node Test Procedure.**
4) Force BTN root creating Configuration 30.
5) Depending on Num_Ports execute test procedure and record results:
   a. Num_Ports = 2: **3 Node Test Procedure.**
   b. Num_Ports > 2: **4 Node Test Procedure.**

6.4.7 Configuration 31

1) Connect configuration as shown in 6.5, Configuration 31.
2) Force PUT to be root.
3) Depending on Num_Ports execute test procedure and record results:
   a. Num_Ports = 2: **4 Node Test Procedure.**
   b. Num_Ports > 2: **5 Node Test Procedure.**

6.5 Small Topology Test Configurations

PUT – PHY under test

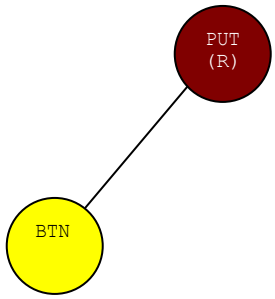
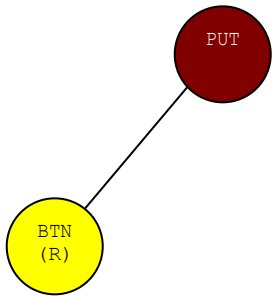
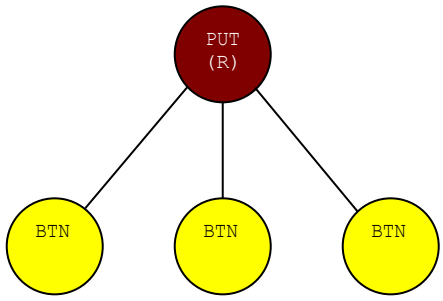
(R) – Root

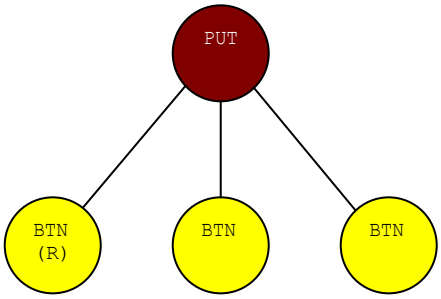
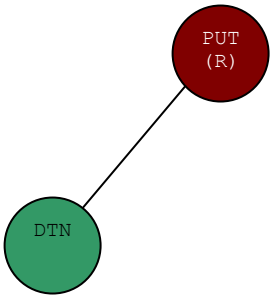
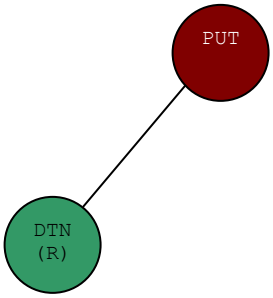
BTN – Beta Test Node

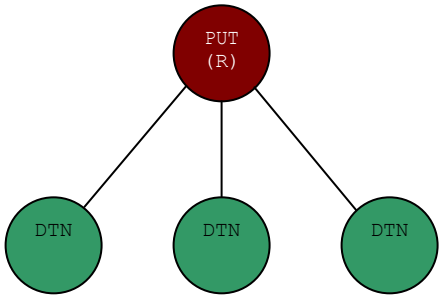
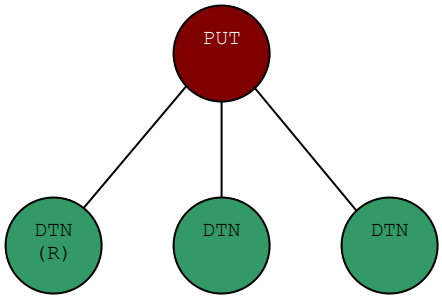
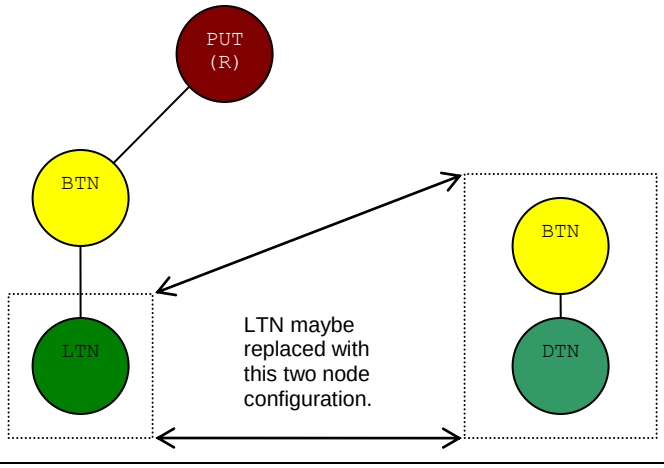
DTN – DS Test Node

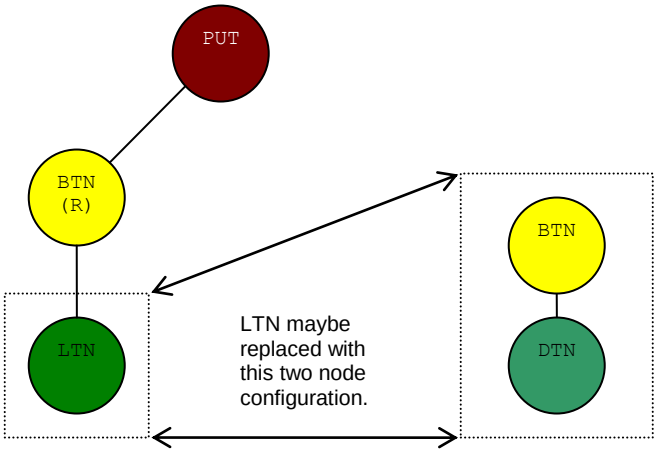
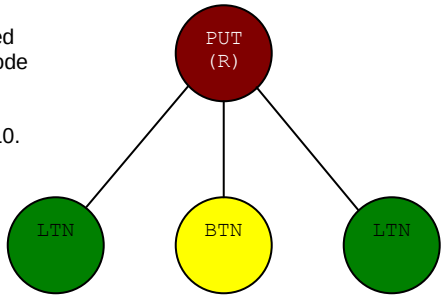
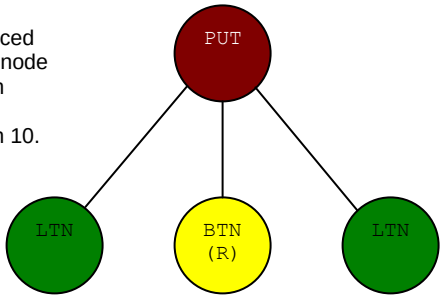
LTN – Beta PHY with Legacy Link (Maximum Speed is S400)

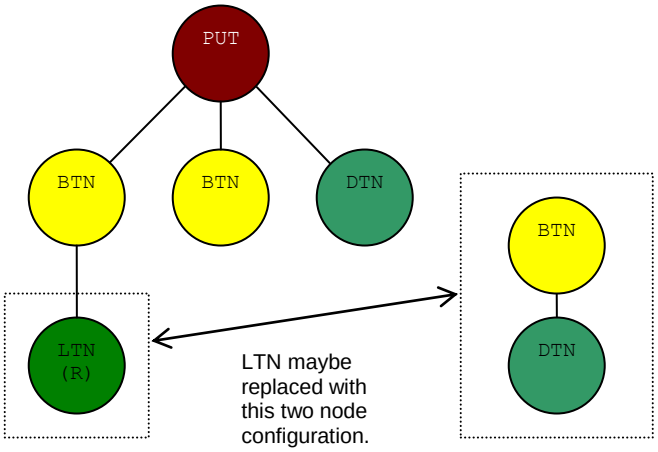
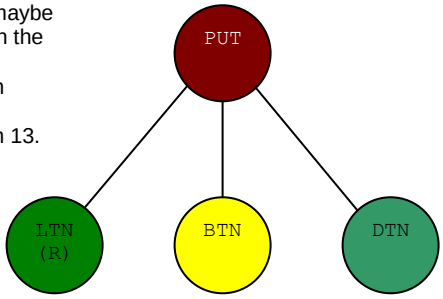
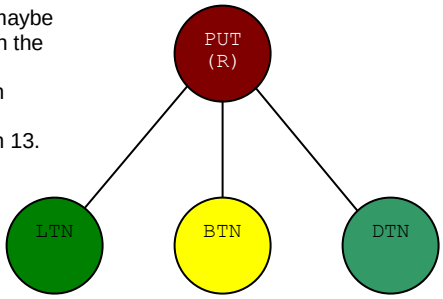
Figure 1: Small Topology Test Configurations.

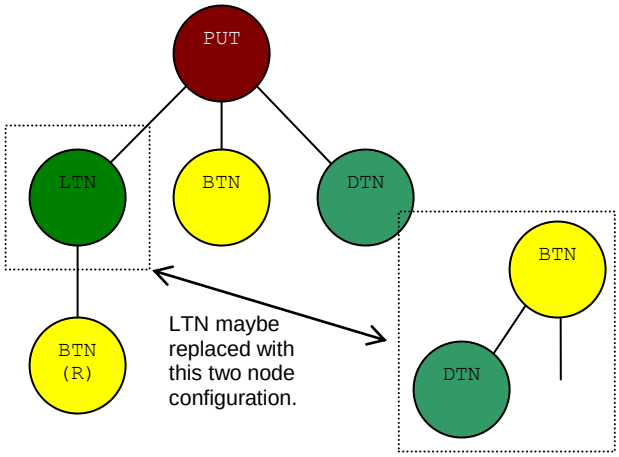
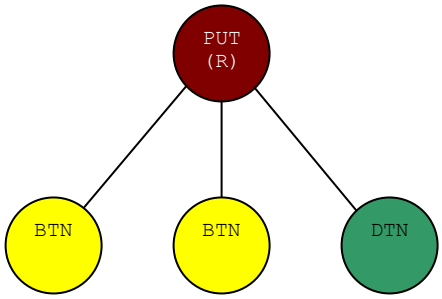
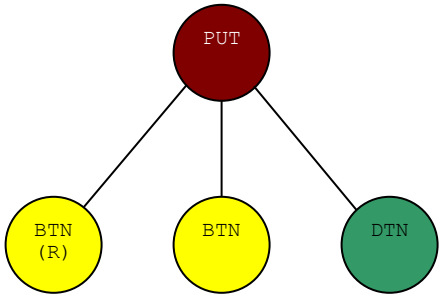
Configuration	DUT Role	Topology
Beta Only Bus		
1	Root (Proxy Root) and Leaf	
2	Non-Root - Leaf	
3	Root (Proxy Root) and Branch	

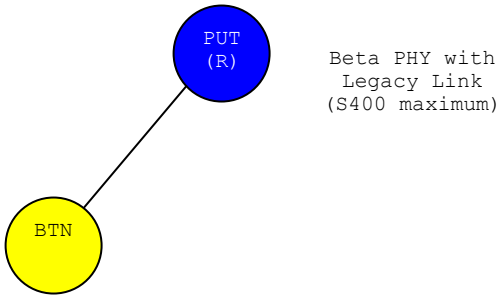
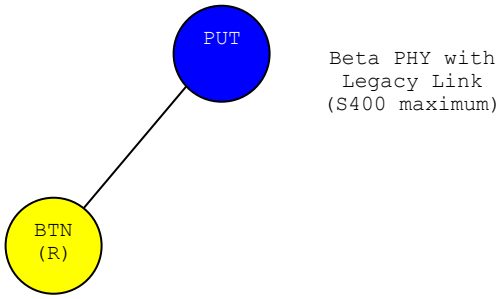
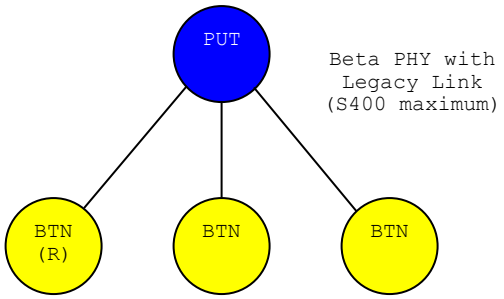
4	Non-Root - Branch	
DS Only		
5	Senior Border – DS Port, B Link, Leaf, Root, Proxy Root	
6	Senior Border – DS Port, B Link, Leaf	

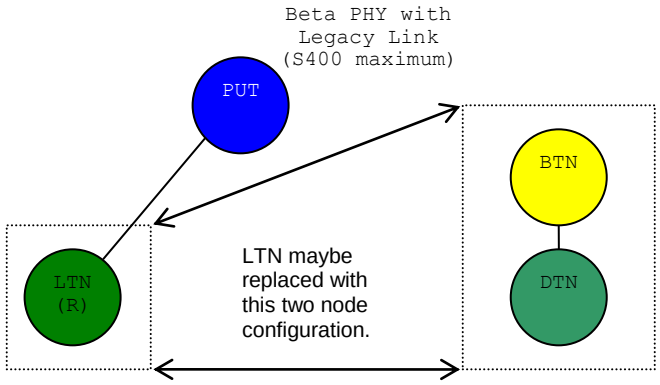
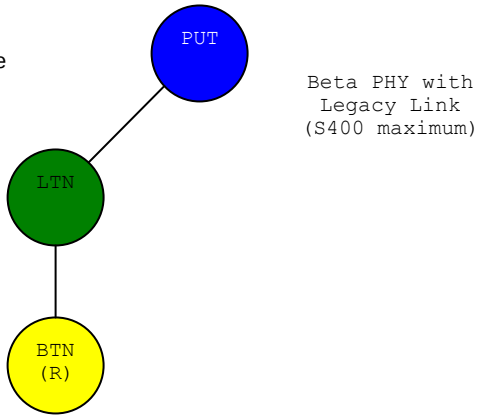
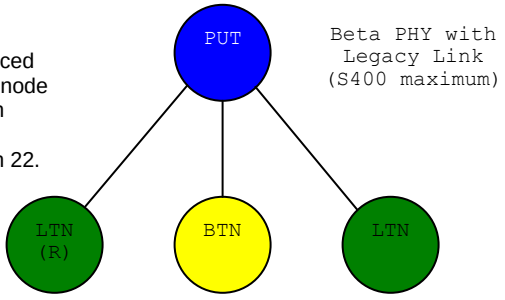
7	Senior Border, Proxy Root and Root – DS Ports, B Link, Branch	
8	Senior Border – DS Ports, B Link, Branch	
	Hybrid Bus with Beta Link	
9	B Node, Leaf - Root	

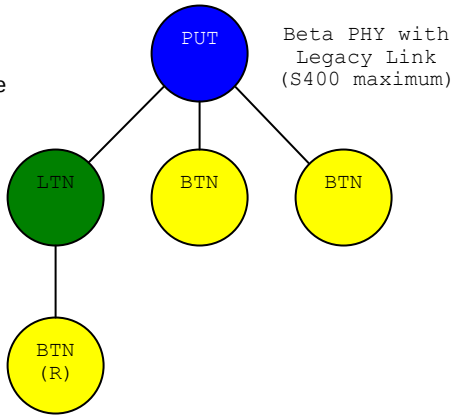
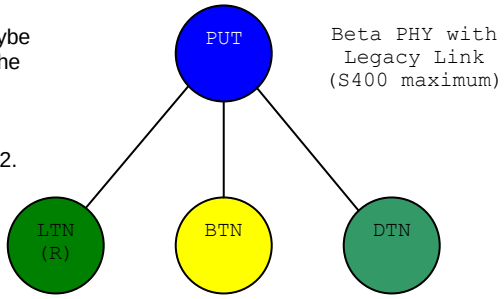
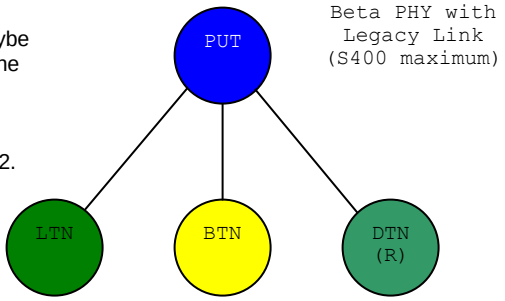
10	B Node, Leaf – non-Root	
11	B Node, Branch – Root, Senior Border, Proxy Root	**Note:** LTNs maybe replaced with the two node configuration shown in configuration 10. 
12	B Node, Branch – non-root, Senior Border, Proxy Root	**Note:** LTNs maybe replaced with the two node configuration shown in configuration 10. 

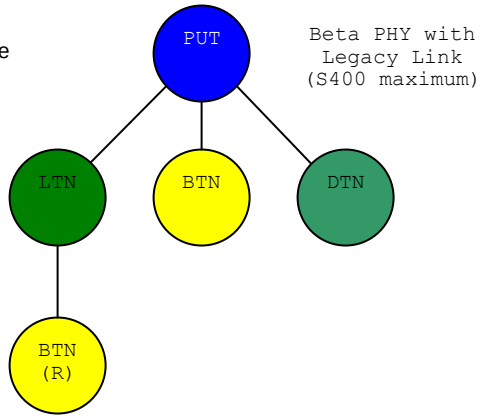
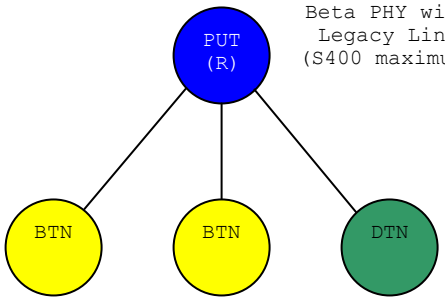
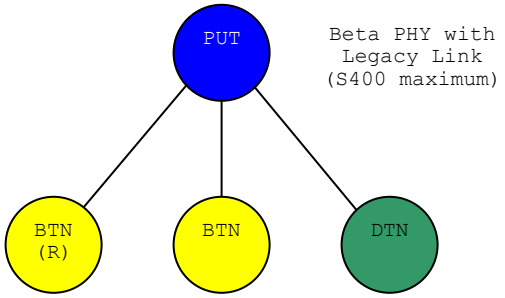
13	Junior Border in Junior Cloud (DS ports, B Link, Branch)	
14	Junior Border – Mixed Ports, B Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 13. 
15	Senior Border, Proxy Root with Junior Border – Mixed Ports, B Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 13. 

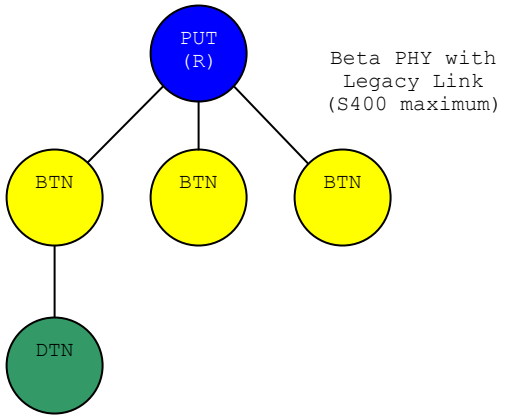
16	Junior Border - B Node Root, Mixed Ports, B Link, Branch	
17	Proxy Root, Senior Border and Root – Mixed Ports, B Link, Branch	
18	Proxy Root and Senior Border – Mixed Ports, B Link, Branch	

Hybrid Bus with Legacy Link		
19	Proxy Root, Senior Border and Root – B Port, Legacy Link, Leaf	
20	Proxy Root, Senior Border – B Port, Legacy Link, Leaf	
21	Proxy Root, Senior Border – B Ports, Legacy Link, Branch	

22	Junior Border – B port, Legacy Link, leaf	
23	Junior Border – B port, Legacy Link, Leaf	**Note:** LTN maybe replaced with the two node configuration shown in configuration 22. 
24	Junior Border – B ports, Legacy Link, Branch	**Note:** LTNs maybe replaced with the two node configuration shown in configuration 22. 

25	Junior Border Root – B Ports, Legacy Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 22. 
26	Junior Border – Mixed Ports, Legacy Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 22. 
27	Proxy Root, Senior Border – Mixed Ports, Legacy Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 22. 

28	Junior Border – Mixed Ports, Legacy Link, Branch	**Note:** LTN maybe replaced with the two node configuration shown in configuration 22. 
29	Proxy Root, Senior Border and Root – Mixed Ports, Legacy Link, Branch	
30	Proxy Root and Senior Border – Mixed Ports, Legacy Link, Branch	

31	Proxy Root and Root – B Ports, Legacy Link, Branch	

7 Large Topology Tests

The following tests are designed to verify the PHY Under Test's (PUT) ability to repeat data through multiple hop topologies. For beta PHYs some topologies test the PHY's ability to break loops and repeat data.

7.1 Loop Tests (Configurations 32-36)

1) Connect configuration as shown in 7.3, Configuration 32 through 36.
2) Execute test **4 Node Test Procedure** and record results.

7.2 Loop Tests (Configurations 37-40)

1) Connect configuration as shown in 7.3, Configuration 37 through 40.
2) Execute test **6 Node Test Procedure** and record results.

7.3 Large Topology Test Configurations

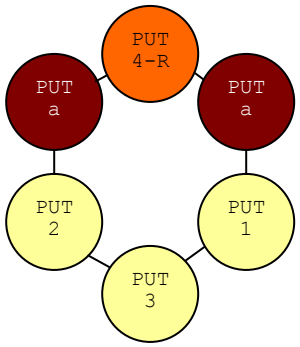
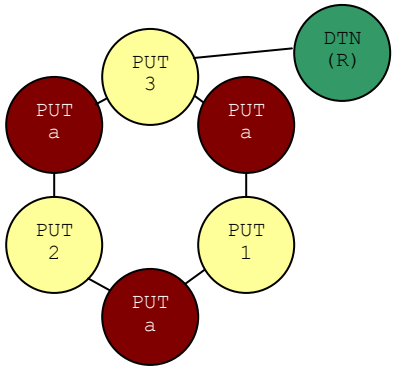
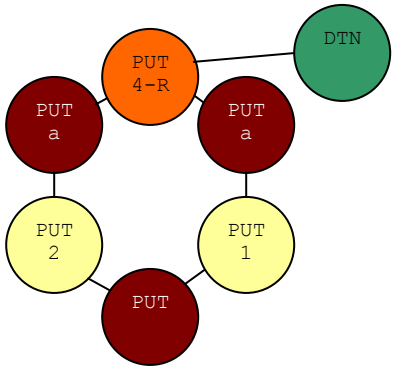
PUT – PHY under test (implies with active link layer)

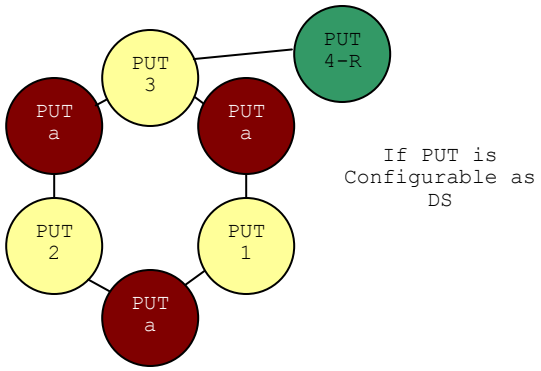
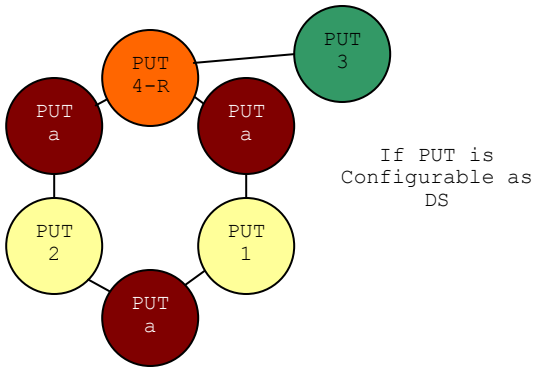
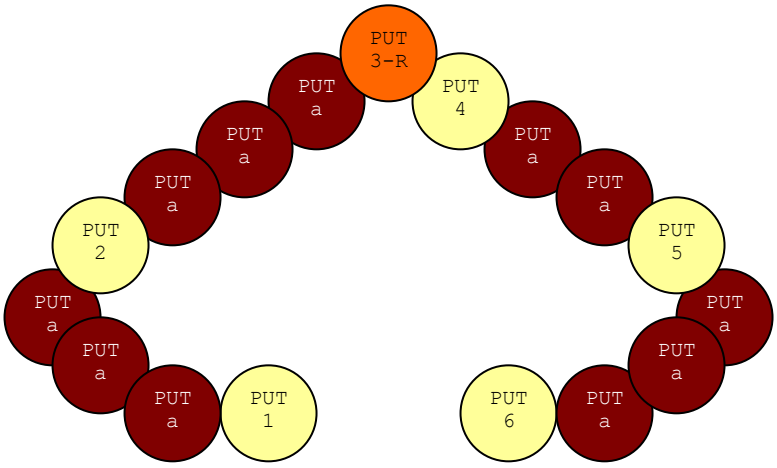
PUTa – PHY under test (link layer may be not active)

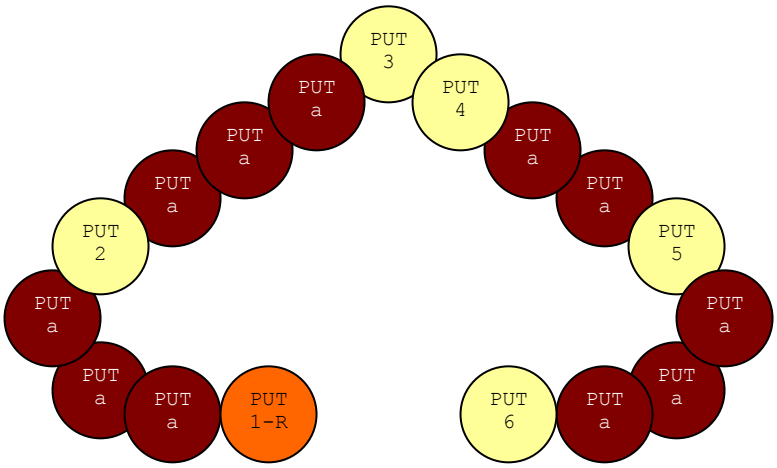
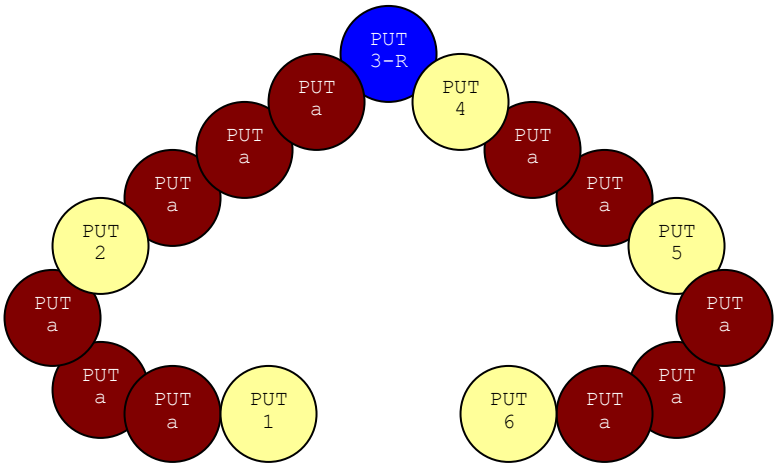
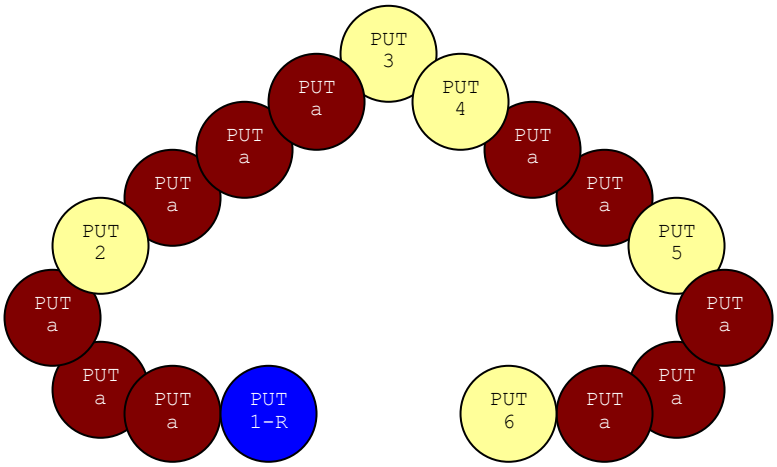
R – Root

Figure 2: Large Topology Test Configurations.

Large Topology (requires 17 PUT, 5 with link)

32	Beta Loop	
33	Beta Loop with Silent DS Leaf Root	
34	Beta Loop and Root with Silent DS Leaf	

35	Beta Loop with Active DS Leaf Root	
36	Beta Root Loop with Active DS	
37	Beta and Root Branch in 17 Node Configuration	

38	Beta and Leaf Root in 17 Node Configuration	
39	DS and Root Branch in 17 Node Configuration	
40	DS and Leaf Root in 17 Node Configuration	

8 Interoperability Tests

This chapter is intended to provide an indication of interoperability between the PHY under test and other PHY's within the industry (Reference PHYs).

8.1 Selection of Reference PHYs

This section defines how to determine reference PHYs. For this test 5 different reference PHYs is required. For some topologies multiple instances of the PHY may be required.

Policy regarding the way to determine reference PHYs:
Select 5 PHY implementations:

Select PHYs according to the following order of priority.

a) Select PHY with 1394 TA compliance logo from other companies.
b) Select PHY from other companies that are (were) available on the market.
c) Select PHY with 1394 TA compliance logo from tester's company.
d) Select PHY from tester's company that are (were) available on the market.

Distribution of the five (5) reference PHYs shall be as follows:

i) Three (3) shall be from the same standard revision as the PHY under test (list standard revision)

- Example: if the PHY under test is a 1394b PHY then 3 of the 5 reference PHYs shall be 1394b

ii) If the PHY under test has at least one bilingual or data/strobe port, one (1) reference PHY shall be a non-suspend and resume (IEEE-1394-1995) PHY. If the PHY under test does not support suspend and resume skip this item.

iii) If the PHY under test has at least one bilingual or data/strobe port, one (1) reference PHY shall be from either IEEE-1394a-2000 or IEEE-1394b-2002 which is not listed in i) above (Example: if the PHY under test is IEEE-1394b-2000 then an IEEE-1394a-2000 reference PHY shall be selected). If the PHY under test does not support suspend and resume one (1) reference PHY from both IEEE-1394a-2000 and IEEE-1394b-2002 shall be selected.

iv) If the PHY under test only supports IEEE-1394b-2002 (it is a beta only PHY) five (5) shall be IEEE-1394b-2002 reference PHYs.

8.2 Data Strobe Tests

For the tests listed in this sections all non-PUT devices shall be replaced with the appropriate test node(s) as determined in 8.1.

Test all tests defined in 6.2.

8.3 Beta Tests

For the tests listed in this sections all non-PUT devices shall be replaced with the appropriate test node(s) as determined in 8.1.

Test all tests defined in 6.1.

8.4 Hybrid Tests

For the tests listed in this sections all non-PUT devices shall be replaced with the appropriate test node(s) as determined in 8.1.

Test all tests defined in 6.3.2.

9 Port Connection Tests

This chapter provides functional tests for the following PHY silicon functionality:

- Suspend and Resume
- Disable and Enable
- Standby and Restore

Other port connection functions are implicitly test through the topology tests specified in this document.

The applicable tests described in this chapter shall be executed twice; once with an IEEE-1394a-2000 test node (TN) and once with an IEEE-1394b-2000 test node (TN).

Select TN PHYs according to the following order of priority.
e) Select PHY with 1394 TA compliance logo from other companies.
f) Select PHY from other companies that are (were) available on the market.
g) Select PHY with 1394 TA compliance logo from tester's company.
h) Select PHY from tester's company that are (were) available on the market.

9.1 Suspend and Resume Tests

Both IEEE-1394a and IEEE-1394b PHY implementations shall implement suspend and resume functionality. This document only attempts to test the suspend and resume functionality initiated through packets and does not attempt to test TpBias related suspend and resume operations such as resume fault or port disconnect.

The following suspend and resume functions have tests defined by this document:

1) PUT sends remote command packet to suspend its port.
   - PUT sends remote command packet to resume its suspended port.
2) TN sends remote command packet to PUT to suspend PUTs port
   - TN resumes its port connected to PUT
3) TN sends remote command packet to suspend its port connected to PUT
   - PUT sends resume packet to resume all suspended ports.

9.2 Disable and Enable Tests

Both IEEE-1394a and IEEE-1394b PHY implementations shall implement disable and enable functionality. For IEEE-1394b PHY implementations this document also defines a Hard Disable port test.

The following disable and enable functions have tests defined in this document:

1) PUT sends remote command packet to disable its port.

- PUT sends remote command packet to enable its disabled port. (Note 1394a PHY will also need to be resumed)

2) TN sends remote command packet to PUT to disable its port connected to the TN.

3) TN sends remote command packet to PUT to disable its port connected a third node.

   - Third node enables its port connected to PUT

4) If PUT is 1394b PHY, set Hard_Disable bit and have PUT send remote command packet to disable its port.

   - Verify no connection status.

   - PUT sends remote command packet to enable its disabled port.

9.3 Standby and Restore Tests

IEEE-1394b PHY implementations shall implement standby and restore functionality.

The following standby and restore functions have tests defined in this document:

1) PUT sends remote command packet to standby its port.

   - PUT sends remote command packet to restore its port that is in standby.

2) TN sends remote command packet to PUT to standby PUTs port

   - TN restores its port connected to PUT

3) PUT sends remote command packet to standby its port.

   - Initiate bus reset and change the bus topology

   - Verify PUT node doesn’t know about bus reset

   - PUT sends remote command packet to restore port in standby

   - Verify PUT node is informed about previous bus reset and bus topology change without further bus resets

10 Test Procedures

10.1 Bus Configuration and Throughput Test Procedures

Bus Traffic Levels

1. Asynchronous only from PUT (no competition)
2. Asynchronous only with competition
3. Asynchronous with competition, cycle starts
4. Cycle starts, isochronous from PUT only
5. Cycle starts, isochronous from TN2 only
6. Cycle starts, isochronous bidirectional
7. Asynchronous from PUT no competition, cycle starts, isochronous from PUT only
8. Asynchronous from PUT no competition, cycle starts, isochronous from TN2 only
9. Asynchronous competition, cycle starts, isochronous from PUT only
10. Asynchronous competition, cycle starts, isochronous from TN2 only
11. Asynchronous competition, cycle starts, isochronous bidirectional

The asynchronous traffic referred to above consists of a series of Write Block Requests followed by Read Block Requests to the same location with the write data being compared with the read data. This process shall be repeated at least 5,000 times per level. This is a single thread. The block transfer packet payload shall be the maximum size allowed for the 1394 bus speed. Single thread with no competition shall consume at least 30% of the buses bandwidth. The actual bandwidth consumed by a single thread with competition will vary; however, the intent is to saturate the 1394bus with multiple threads running.

The isochronous stream referred to above consists of a stream with maximum size payload allowed for the 1394 bus speed or that the sum of all streams does not exceed 80% bus utilization. For levels 4. through 6. the isochronous stream(s) shall run continuously for at least 20 second per level. For levels 9. through 11. the isochronous stream(s) shall run continuously for the duration of the asynchronous traffic.

10.1.1 Point-to-Point Test Procedure

The incremental nature of this test procedure is intended to help debug the root cause of any issue encountered during the test. The tester may skip levels 1 through 10 and only execute level 11. However if this approach is used then level 11 should be run 4 times or for 4 times the duration.

1) Create and verify the bus topology
2) If PHY is 1394a or 1394b PHY:
   - Set Enab_accel and Enab_multi to false
   - Set Link_active to true
   - Set 1394aorb node variable to true

   else PHY is IEEE-1394-1995 PHY:
   - Set 1394aorb node variable to false
3) Execute Level 1: asynchronous requests only from PUT to TN2
4) Verify Level 1 test results
5) Execute Level 2: asynchronous requests from PUT to TN2 and TN2 to PUT
6) Verify Level 2 test results
7) Enable cycle master
8) Execute Level 3: asynchronous requests from PUT to TN2 and TN2 to PUT
9) Verify Level 3 test results

10) Execute Level 4: isochronous stream from PUT to TN2
11) Verify Level 4 test results
12) Execute Level 5: isochronous stream from TN2 to PUT
13) Verify Level 5 test results
14) Execute Level 6: isochronous stream from PUT to TN2 and TN2 to PUT
15) Verify Level 6 test results
16) Execute Level 7: asynchronous from PUT no competition, cycle starts, isochronous from PUT only
17) Verify Level 7 test results
18) Execute Level 8: asynchronous from PUT no competition, cycle starts, isochronous from TN2 only
19) Verify Level 8 test results
20) Execute Level 9: asynchronous competition, cycle starts, isochronous from PUT only
21) Verify Level 9 test results
22) Execute Level 10: asynchronous competition, cycle starts, isochronous from TN2 only
23) Verify Level 10 test results
24) Execute Level 11: asynchronous competition, cycle starts, isochronous bidirectional
25) Verify Level 11 test results
26) If executing level 11 only repeat steps 24) and 25) four times

10.1.2 Three Node Test Procedure

1) Execute Point-to-Point Test Procedure between TN1 and PUT.
2) Execute Point-to-Point Test Procedure between TN2 and PUT.
3) Verify and record results.

10.1.3 4 Node Test Procedure

1) Execute Point-to-Point Test Procedure between TN1 and PUT.
2) Execute Point-to-Point Test Procedure between TN2 and TN3.
3) Verify and record results.

10.1.4 5 Node Test Procedure

1) Execute Point-to-Point Test Procedure between TN1 and PUT.
2) Execute Point-to-Point Test Procedure between TN2 and TN3.
3) Execute Point-to-Point Test Procedure between TN4 and PUT.
4) Verify and record results.

10.1.5 6 Node Test Procedure

1) Execute Point-to-Point Test Procedure between PUT1 and PUT6.
2) Execute Point-to-Point Test Procedure between PUT2 and PUT4.
3) Execute Point-to-Point Test Procedure between PUT3 and PUT5.
4) Verify and record results.

10.2 Port Configuration Test Procedure

10.2.1 Suspend and Resume Test Procedure

10.2.1.1 1394a Suspend and Resume Test Procedure

If PUT is a 1394a or bilingual PHY or PUT has 1394a ports execute the following test:

1) Connect PUT directly to 1394a TN

2) Suspend PUT’s port connected to TN with a remote command packet sent from PUT to PUT

3) Verify bus reset occurs and PUT and TN see single node topology

4) Resume PUT's port connected to TN with a remote command packet sent from PUT to PUT

5) Verify bus reset occurs and PUT and TN see two node topology

6) Suspend PUT's port connected to TN with a remote command packet sent from TN to PUT

7) Verify bus reset occurs and PUT and TN see single node topology

8) Resume TN's port connected to PUT with a remote command packet sent from TN to TN

9) Verify bus reset occurs and PUT and TN see two node topology

10) Connect all PUT ports to 1394a TN

10) Suspend TN's port connected to PUT with a remote command packet sent from PUT to TN

11) Verify bus reset occurs and PUT and all TNs see single node topology

12) Resume PUT's port connected to all TNs with resume packet to resume all ports sent from PUT to PUT

13) Verify bus reset occurs and PUT and TNs see correct number of nodes in topology

10.2.1.2 1394b Suspend and Resume Test Procedure

If PUT is a 1394b PHY or has 1394b ports execute the following test:

1) Connect PUT directly to 1394b TN

2) Suspend PUT's port connected to TN with a remote command packet sent from PUT to PUT

3) Verify bus reset occurs and PUT and TN see single node topology

4) Resume PUT's port connected to TN with a remote command packet sent from PUT to PUT

5) Verify bus reset occurs and PUT and TN see two node topology

6) Suspend PUT's port connected to TN with a remote command packet sent from TN to PUT

7) Verify bus reset occurs and PUT and TN see single node topology

8) Resume TN's port connected to PUT with a remote command packet sent from TN to TN

9) Verify bus reset occurs and PUT and TN see two node topology

10) Connect all PUT ports to 1394a TN

11) Suspend TN's port connected to PUT with a remote command packet sent from PUT to TN

12) Verify bus reset occurs and PUT and all TNs see single node topology

13) Resume PUT's port connected to all TNs with resume packet to resume all ports sent from PUT to PUT

14) Verify bus reset occurs and PUT and TNs see correct number of nodes in topology

15) Repeat steps 1) through 9) for all ports

10.2.2 Disable and Enable Test Procedure

10.2.2.1 1394a Disable and Enable Test Procedure

If PUT is a 1394a or bilingual PHY or PUT has 1394a ports execute the following test:

1) Connect PUT directly to 1394a TN

2) Disable PUT's port connected to TN with a remote command packet sent from PUT to PUT

3) Verify bus reset occurs and PUT and TN see single node topology

4) Enable PUT's port connected to TN with a remote command packet sent from PUT to PUT

5) Verify no bus reset occurs and PUT and TN see one node topology

6) Resume PUT's port connected to TN with a remote command packet sent from PUT to PUT

7) Try to disable PUT's port connected to TN with a remote command packet sent from TN to PUT

8) Verify no bus reset occurs and PUT and TN still see a two node topology

9) If PUT has more than one port connect a second port to a second 1394a TN (TN2)

10) Disable PUT's port connected to TN2 with a remote command packet sent from TN to PUT

11) Verify bus reset occurs and PUT and TN see two node topology while TN2 sees single node topology

12) Enable PUT's port connected to TN2 with a remote command packet sent from TN to PUT

13) Verify no bus reset occurs and PUT and TN see two node topology

14) Resume PUT's port connected to TN2 with a remote command packet sent from PUT to PUT

15) Verify bus reset occurs and three node topology is observed by all nodes

10.2.2.2 1394b Disable and Enable Test Procedure

If PUT is a 1394b PHY or has 1394b ports execute the following test:

1) Connect PUT directly to 1394b TN

2) Disable PUT's port connected to TN with a remote command packet sent from PUT to PUT

3) Verify bus reset occurs and PUT and TN see single node topology

4) Enable PUT's port connected to TN with a remote command packet sent from PUT to PUT

5) Verify bus reset occurs and PUT and TN see two node topology

6) Try to disable PUT's port connected to TN with a remote command packet sent from TN to PUT

7) Verify no bus reset occurs and PUT and TN still see a two node topology

8) If PUT has more than one port connect a second port to a second 1394a TN (TN2)

10) Disable PUT's port connected to TN2 with a remote command packet sent from TN to PUT

11) Verify bus reset occurs and PUT and TN see two node topology while TN2 sees single node topology

12) Enable PUT's port connected to TN2 with a remote command packet sent from TN to PUT

13) Verify bus reset occurs and three node topology is observed by all nodes

10.2.3 Standby and Restore Test Procedure

If PUT is a 1394b PHY or has 1394b ports execute the following test:

1) Connect PUT directly to 1394b TN

2) Standby PUT's port connected to TN with a remote command packet sent from PUT to PUT

3) Verify no bus reset occurs and PUT and TN see two node topology

4) Restore PUT's port connected to TN with a remote command packet sent from PUT to PUT

5) Verify no bus reset occurs and PUT and TN see two node topology

6) Standby PUT's port connected to TN with a remote command packet sent from TN to PUT

7) Verify no bus reset occurs and PUT and TN see two node topology

8) Restore PUT's port connected to TN with a remote command packet sent from PUT to PUT

9) Verify no bus reset occurs and PUT and TN see two node topology

10) Connect a second TN (TN2) to TN and force TN root

11) Standby PUT's port connected to TN with a remote command packet sent from TN to PUT (PUT is nephew and TN is uncle)

12) Verify no bus reset occurs and PUT still sees a three node topology

13) Change the bus topology of TN and TN2 by forcing root TN2 to be root.

14) Verify no bus reset occurs at PUT and PUT only sees original three node topology

14) Restore PUT's port connected to TN with a remote command packet sent from PUT to PUT

15) Verify no bus reset occurs and PUT receives the update bus information

16) Connect a second TN (TN2) to PUT and force PUT root

11) Standby TN's port connected to PUT with a remote command packet sent from PUT to TN (PUT is uncle and TN is nephew)

12) Verify no bus reset occurs and PUT still sees a three node topology

13) Change the bus topology of PUT and TN2 by forcing root TN2 to be root.

14) Verify bus reset occurs at PUT and PUT sees new three node topology

14) Restore PUT's port connected to TN with a remote command packet sent from PUT to PUT

15) Verify no bus reset occurs and PUT and TN receives the update bus information

Annex A
(informative)

Bibliography

[B1] IEEE Std 1212-2001, Standard for a Control and Status Registers (CSR) Architecture for microcomputer buses

[B2] IEEE Std 1394-1995, Standard for a High Performance Serial Bus

[B3] IEEE Std 1394a-2000, Standard for a High Performance Serial Bus—Amendment 1

[B4] IEEE Std 1394b-2002, Standard for a High Performance Serial Bus—Amendment 2

[B5] ISO/IEC 9899:1990, Programming Languages—C