IEEE-1394 and AS5643 bring deterministic networking to high reliability Mil-Aero designs

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For years, IEEE-1394 (FireWire) has been a successful and popular consumer electronics and computer interface. While that is true, the strongest design activity recently has been in other sectors. Over the past 17 years IEEE-1394 has been gaining traction as an aerospace and defense (A&D) high-speed interface and is used in programs such as the F-35 Lightning II, NPOESS, X47B, JSOW, and X2000, plus many others.

Much of IEEE-1394's success came with the development of IEEE-1394b-2002, which specified several key features that when coupled with SAE Standard AS5643 created a deterministic, robust, and redundant system architecture that meets most A&D requirements for a hard real-time control bus. Technology suitability studies are common within the A&D industry for specific subsystems such as flight control, mission systems, and avionics to measure how technology meets stringent requirements; this document highlights several criteria often used to evaluate I/O technologies an how 1394 coupled with AS5643 meet them.

IEEE-1394 was first standardized in 1995. Major updates were completed in 2000 (IEEE-1394a-2000), 2002 (IEEE-1394b-2002), and in 2008 (IEEE-1394-2008). IEEE-1394-2008 Beta refined and extended IEEE-1394b-2002. It defines operation from S100 (98.304 Mb/s) to S3200 (3.932 Gb/s). Given this wide range of throughput options, 1394 is suitable for vehicle management and avionic and mission system networks including Electro-Optic/Infrared (EO/IR) sensor interfaces.

Deterministic behavior, excellent "robustness"
AS5643 coupled with IEEE-1394 Asynchronous Stream capability provides a programmable rate-based (time-sliced) protocol. The rate is determined by a control computer - also known as a Vehicle Management Computer (VMC) - generated Start of Frame (STOF) packet. Using pre-assigned offsets, each device can determine when to have data ready for transmission and also when to expect data from the bus. This allows for deterministic operation from the 1394 bus through each device and through the complete network.

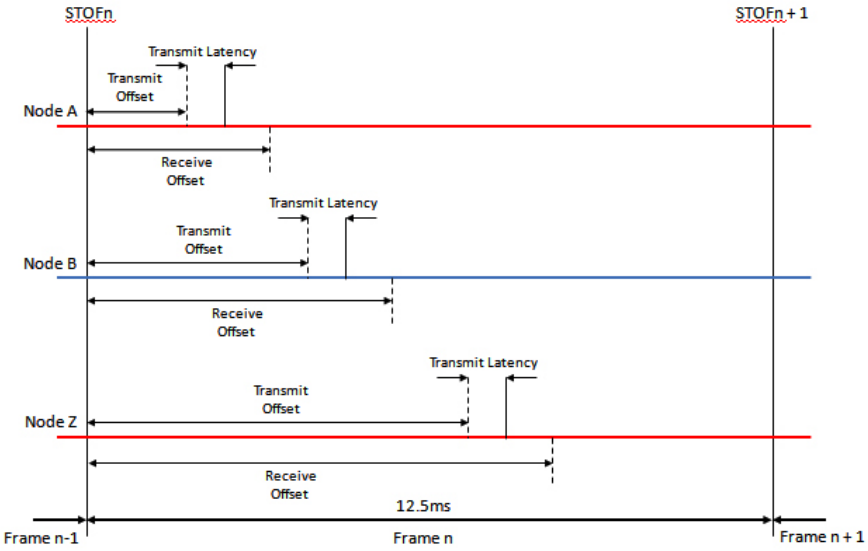

Figure 1: AS5643 Rate Based (TDMA-style) Deterministic Timing

In addition, AS5643 takes full advantage of IEEE-1394-2008 beta's scrambled 8b10b encoding,

which allows for transformer, capacitor, and optical isolation. Both transformer and fiber optic isolated systems have been tested to meet RTCA/DO-160 lightening susceptibility requirements.

Fault tolerance
AS5643 takes advantage of a 1394-2008 beta feature - looped topologies. 1394-2008 beta supports point-to-point, daisy chain, treed and multiple loop topologies. AS5643 recommends using loops to create a first level of topology fault tolerance, then defines a second level using double or even triple redundant networks. In addition to fault tolerance through the network architecture, 1394-defined header and data cyclic redundancy check (CRC) and AS5643-defined vertical parity check (VPC) provide bus level and application level error detection respectively.

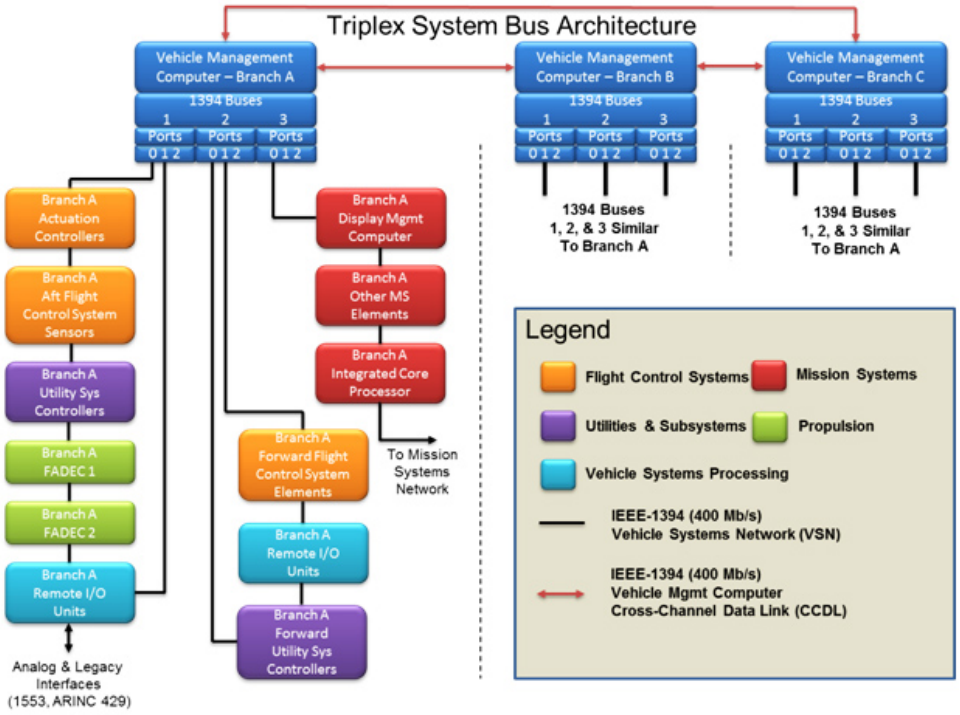

Figure 2: Triplex System Bus Architecture

Other Key Benefits
Initialization Time –IEEE-1394-2008 beta has a power-up initialization time of approximately 500msec, while a long bus reset plus topology configuration takes approximately 200usec for a nominally-sized bus. Both of these times are considered more than acceptable for most A&D applications. AS5643 also applies an initialization saving technique of pre-assigning channel addresses, thus creating a no node re-discovery requirement after bus resets. This not only saves initialization time but also reduces software complexity and increases network robustness.

Risk (maturity)– IEEE-1394 is a mature technology. Billions of commercial products with FireWire have shipped over the past 17 years. Originally approved by the SAE in 2004, AS5643 together with IEEE-1394 is flying in multiple aircraft, including the F35 Lightening II and X47B UCAS, plus others.

COTS– Benefiting from years of development and commercial applications,most 1394 A&D applications today use COTS silicon. For example, the same 1394 Open Host Controller Interface (OHCI) implementations used in Macs or PCs are used for control computer implementations. This has reduced direct product costs and also has allowed A&D to take full advantage of the existing 1394 ecosystem such as chipsets, IP-cores, software stacks, test and measurement equipment, and manufacturing test systems.

Weight and Volume– IEEE-1394-2008 beta requires two differential pairs per port, or one TX/one RX per fiber optic port. 1394's flexible cable topology support (homerun cabling is not required like star or switched architectures) allows the system implementer to optimize cable routing to meet weight/volume and robustness requirements.

Power Consumption– IEEE-1394-2008 beta requires two LVDS-type differential pairs per port. Using common 8b10b signaling, beta 1394 can be implemented with power/performance optimized SERDES implementations. The digital logic in most S400 PHY and Link implementations operates at less than 50MHz, which reduces switching currents.

Software Requirements –AS5643's architecture applies several techniques to reduce software requirements and increase robustness. Specifically, pre-assigned addresses eliminate device discovery and allow for hardware address filtering. While frame rate and offset times may be programmable, most system implementations fix these times, allowing for optimized device implementations.

Scalability – A&D life cycles can often last multiple decades. IEEE-1394 is architected to scale in data rate with minimal software and cable harness changes. Implemented using common SERDES technology IEEE-1394-2008 beta is FPGA-friendly, with multiple IP cores available. This has the effect of future- proofing 1394 when it's used in long term A&D applications.

Cable Length –Often these applications feature considerable distances between nodes. According to Gore's Quadrax cable selection guide for AS5643, 24 meters at S400 is possible with active transformers, and 50 meters is possible at S100 with active transformers. Cable length may be extended even further using repeaters or fiber optics.

The sum is greater than the parts

This list of features undoubtedly indicates AS5643/1394's suitability for many A&D deterministic applications. However, when looked at from a system view AS5643/IEEE-1394-2008 Beta is an ideal solution for safety-critical, deterministic (hard real-time) distributed control. As such, it provides the guaranteed latency and jitter needed to ensure that the data required for distributed control functions is delivered in a timely and predictable manner.

The use of a predefined message schedule with a distributed frame rate provides known and exactly predictable communication bus loading and message sequencing.

AS5643's use of looped topologies and redundant bus architecture means that the failure of a single node, or even several nodes, does not prevent synchronized communication from continuing between the remaining nodes. Fault detection, containment, and tolerance are provided via the voting protocol, message status, application level consistency checks, and data integrity checks implemented in the hardware.

AS5643/1394 supports hot swap of nodes on the network. Faulty nodes can be replaced and new nodes integrated without powering down the rest of the system. This along with the strict interface specification supports modularity in system upgrades and new system integration. Modules can be upgraded and swapped with existing modules without disturbing the system and without full-system requalification. The strict interface definition allows different manufacturers to create modules and essentially guarantees successful integration if the interface definitions are enforced.

The communication rates supported by AS5643/1394 hardware currently available are suitable for the real-time control requirements of all safety critical vehicle subsystems. Higher data rates are only needed if noncritical data is transmitted along with critical data. However, if higher speed transmission is required 1394's layered architecture is obtained by moving to an appropriate physical layer.

Finally, AS5643/1394 represents a cost-effective solution. Capitalizing on 1394's commercial success, control computer and remote node chipsets, IP Cores and supporting development software are commercially available at a reasonable cost. The communication controller can be implemented in a radiation-tolerant FPGA or in a radiation-hardened ASIC device for deployment if needed.

Implementation of the protocol in the hardware, such as transmit frame offset timing support, reduces the complexity and cost of software development. Unlike switched technologies, homerun cabling is not required to reach obscured devices, while support for both copper and fiber optics provides the option to network nodes at long distances. This reduces long runs of bulky wiring bundles by placing the nodes close to the system components being monitored and controlled. 1394's treed/loop topology support allows the wiring connections to multiple sensors and actuators to be shortened - only the lightweight twisted pair buses will be routed over significant lengths.

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